REMARKS

Applicants respectfully traverse and request reconsideration. Applicants would like to thank the Examiner for allowing claim 40 and for indicating that claims 7–12, 14, and 16–17, would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 2, 7–12, 14, 15, and 20 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim Applicants' subject matter. Applicants have previously corrected the typographical error in claim 2 in the previous response to the Office Action dated April 9, 2003. As a result of the previous amendment, the limitation "the second internal signal" in claim 2's third line has support from claim 2's second line as "a second internal signal."

Claims 1–6, 13, 15, and 18–39 currently stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,141,021 (Bickford et al.).

Bickford

Bickford is directed to a device to disable a graphics process for avoiding bus contention on an accelerator graphics port (AGP) (Bickford ¶ 1, lines 5-8.). A disable device 124 selectively disables either the video down AGP graphics accelerator 118 or the add-in AGP card 122 (Bickford ¶ 4, lines 46–49). Thus, two AGP accelerators 118, 122 may be *simultaneously coupled to the AGP 110* since the disabled device 124 disables one of the AGP graphics accelerators 118, 122 and prevents both devices 118, 122 from contending for the AGP 110 (Bickford ¶ 4, lines 49–53, emphasis added). Accordingly, Bickford requires that both AGP 118 and add-in AGP 122 receive the same signals from the AGP bus 110.

It is well established that to establish *prima facie* obviousness, all the claim limitations must be taught or suggested by the prior art. In addition, there must be some teaching, motivation or suggestion in either the prior art, or the references themselves to make the combination asserted by the Examiner. In reviewing the Office Action, the Examiner asserts "it would have been obvious to skilled in the art to modify the system of Bickford to add an input buffer to" enhance the graphical processing capability.

Measuring a claimed invention against the standard established in § 103 requires the oft-difficult but critical step of casting the mind back to the time of invention, to consider the thinking of one of ordinary skill in the art, guided only by the prior art references in the then-accepted wisdom in the field. Close adherence to this methodology is especially important in the case of less technologically complex inventions, where the very ease with which the invention can be understood may prompt one "to fall victim to the insidious effect of a hindsight syndrome wherein that which only the inventor taught is used against its teacher."

Case law makes it clear that the best defense against the subtle but powerful attraction of a hindsight-based obviousness analysis is rigorous application of the requirement for a showing of the teaching or motivation to combine prior art references. Combining prior art references without evidence of such a suggestion, teaching or motivation simply takes the inventor's disclosure as a blueprint for piecing together the prior art to defeat patentability—the essence of hindsight. Evidence of a suggestion, teaching or motivation to combine may flow from the prior art references themselves, the knowledge of one of ordinary skill in the art, or, in some cases, from the nature of the problem to be solved, although "the suggestion more often comes from the teachings of the pertinent references." ("The Board must identify specifically . . . the reasons one of ordinary skill in the art would have been motivated to select the references and combine them.") The showing of such suggestion, teaching, or motivation must be clear and particular. Broad, conclusory statements regarding the teaching of multiple references, standing alone, are not "evidence."

The Office Action acknowledges that Bickford does not explicitly disclose an input buffer to receive the external signals. However, the Office Action asserts that "it is a common industrial practice in the computer art to equip an input buffer with the AGP." Further, the Office Action asserts that "it would have been obvious to one having ordinary skill in the computer art to modify Bickford with common industrial practice at the time Applicant made the invention to enhance the graphical processing capability." With regard to the Examiner's assertion of the motivation of one skilled in the art to modify the system of Bickford, a careful examination of Bickford as cited reveals that Bickford teaches simultaneously coupling the graphics accelerators 118, 122 to the AGP bus 110 and disabling one of the AGP graphic accelerators 118, 122 to prevent both devices 118, 122 from contending for the AGP 110

(Bickford ¶ 4, lines 49-53). Accordingly, Bickford would have no need to add an input buffer, since the disabled device 124 already enables and disables the AGP graphics accelerators 118, 122 in order to avoid bus contention on the AGP bus 110. Modifying Bickford to include an input buffer would result in adding redundant hardware. Further, adding hardware may cause signaling delays in the AGP bus due to signal propagation delays through the input buffer, which may reduce the operating speed of the AGP bus 110. Accordingly, such modification as suggested in the Office Action would reduce, rather than enhance, the graphical processing capability of Bickford, since Bickford seeks to avoid bus contention or increase the bus speed (Bickford ¶ 1, lines 39-50).

Bickford teaches resolving a completely different problem than the claim. Bickford as stated above teaches resolving bus contention, whereas the claims recite an "input buffer operable to receive a first external signal via a first external signal path." Accordingly, since Bickford teaches avoiding bus contention through the use of coupling the AGP graphics accelerators 118, 122 simultaneously to the AGP bus 110, and disabling one of the AGP graphic accelerators 118, 122 through a disable device 124, Bickford teaches away from the claims because adding an input buffer to the AGP graphic accelerators 118, 122 would reduce the performance of the AGP bus 110 and add extraneous hardware that would provide a function redundant to the disable device 124 for avoiding bus contention.[1]

BICKFORD FAILS TO DESCRIBE A FIRST INTERNAL SIGNAL PATH AND A FIRST EXTERNAL SIGNAL PATH

Secondly, according to the Office Action, the claimed first internal signal path corresponds to the path connecting AGP graphics accelerator 118 and AGP bus 110, and the claimed first external path corresponds to the path connecting structures AGP bus 110 and AGP add-in card connector 120 as shown in Figure 3. However, the path connecting structures 118 and 110, and the path connecting structures 110 and 120 are the same path, namely AGP 110, as also shown in Figure 3. Unlike the claims, these paths in Bickford are not separate paths as claimed, but the same path, as acknowledged in the Office Action as AGP 110. The Office

[1] A prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention. *W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), *cert. denied*, 469 U.S. 851 (1984), MPEP 2141.02.

Action also improperly refers to the AGP 110 to describe the internal and external paths (referring to structures 118 and 110, and 110 and 120). However, the claims require separate paths, namely, a first internal signal path and a first external signal path where the input buffer is operable to receive the first external signal via the first external signal path. Accordingly, the first internal signal path is distinct from the first external signal path.

Thirdly, according to the Office Action on page 11 paragraph reference no. 11, Bickford has one internal path and one external path. However, AGP bus 110 cannot be both external and internal at the same time. In other words, AGP bus 110 cannot be both internal to itself and external to itself as would be required based on the assertion of the Office Action that AGP bus 110 functions both as the internal data path and the external data path. Further, by asserting that an AGP bus functions both as an internal data path and external data path, the Office Action ignores the difference between the claimed external and internal data paths. Further yet, such an assertion obliterates the distinction between the first external signal and the second internal signals as claimed. For example, a first internal signal and a first external signal cannot simultaneously exist on a bus 110, since bus 110 can only at any point in time carry one signal and not two signals such as the first internal signal and the first external signal. Accordingly, the Office Action requires that the first internal signal and the first external signal are always the same unlike the claims.

As to claim 1, for example, Applicants claim a first internal circuit, such as an internal bus bridge or internal graphics processor, that provides a first internal signal via an internal signal path. An input buffer is operable to receive a first external signal, such as from an external graphics processor, via an external signal path. A selector circuit is coupled to both the first internal circuit and to the input buffer. The selector circuit is coupled to the first internal circuit via the internal signal path and is operable to select either the first internal signal or the external signal to provide a selected signal. As such, among other advantages, the input buffer isolates the external signal path from the first internal circuit. No such input buffer, first external path, or selector circuit as arranged in the claims is taught or suggested by the cited reference and, as such, the rejection is improper.

Fourthly, Bickford as cited teaches the use of a conventional bus architecture so that "devices on the bus can send and receive information from other devices." (Bickford col. 1, lines 19-20.) Accordingly, a motherboard includes an AGP graphics accelerator chip 118 coupled to the accelerated graphics port (AGP) 110. (Bickford col. 4, lines 41-44.) Bickford also requires a connector 120 coupled to the AGP 110 that is adapted to receive an AGP graphics accelerator add-in card 122. As a result, Bickford does not teach a first external signal path because Bickford teaches, "A connector 120 adapted to receive an *AGP graphics accelerator add-in card 122 is coupled to the AGP 110*, along with a device 124 for selectively disabling either on board AGP graphics accelerator 118 or the add-in AGP card seated 122 in the connector 120." (Emphasis added.) Therefore, unlike the claims, Bickford teaches that the same AGP 100 is always coupled to both the onboard AGP graphics accelerator chip 118 and the add-in card 122. As previously stated, the claims require separate paths, namely a first internal signal path and a first external signal path where the input buffer is operable to receive the first external signal via the first external signal path. As a result, since the connector 120 is directly coupled to the AGP, Bickford does not teach, and further teaches against, a first internal and a first external path. Consequently, Bickford teaches against a first internal signal path and a first external signal path where the input buffer is operable to receive the first external signal via the first external signal path. Therefore, since Bickford as cited teaches against the claims, the Office Action fails to establish a *prima facie* case of obviousness.

Fifthly, because Bickford fails to teach an input buffer and an external signal path, Bickford also fails to teach coupling the first external signal path to the input buffer. Rather, AGP graphics accelerators 118, 122 are both coupled to the same AGP 110. (*Id.*) Bickford also teaches against the claims because Bickford teaches coupling the first external signal path to the first internal signal path. Again, rather than teaching coupling the first external signal path to the input buffer, Bickford is directed to a completely different problem and does not address the problems sought to be overcome. For example, the Bickford reference is silent as to addressing echoes or signal reflections on transmission lines from expansion slots for an external graphics controller card, and, in fact, teaches away from addressing the problem, since all embodiments appear to be shown with the AGP bus 110 being coupled directly to the AGP add-in card connector or to the AGP controller. As previously stated, the Bickford reference teaches enabling and disabling the AGP graphics accelerators 118, 122 and therefore uses a completely

different approach from that claimed by Applicants. The Bickford reference suffers from the same problems described in Applicants' "Background of the Invention" section since the expansion slot AGP bus lines of Bickford are not isolated, but instead are coupled to the AGP 110 as with conventional configurations. In contrast, Applicants' invention addresses the problem of echoes or signal reflections from an expansion slot that can interfere with on chip graphics controllers' reception of signals. Accordingly, Bickford teaches away from the claims.

Sixthly, since the Office Action acknowledges that Bickford does not disclose the claimed input buffer, the corresponding combination of structure with respect to the selector circuit and first internal circuit is also not disclosed. The Office Action takes official notice that it is common practice to allegedly use an input buffer with the AGP as claimed. Applicants respectfully note, as stated above, that Bickford teaches away from using Applicants' claimed input buffer by showing that the AGP bus 110 and the expansion slot 118 or onboard AGP graphics adapter 122 are directly coupled. In fact, Bickford uses a completely different approach. As previously stated, Bickford teaches a conventional bus architecture coupled to peripheral devices and enabling and disabling the peripheral devices, such as AGP graphics accelerators 118, 122. As a result, Bickford teaches against the use of a first external path, an input buffer, and a selector circuit as previously stated. Bickford teaches the common practice of a conventional bus architecture coupled to peripheral devices and enabling and disabling the peripheral devices. This common practice teaches against the claims. Consequently, the assertion that the common practice is to use an input buffer with the AGP as claimed is unsupported and incorrect, especially in view of the teachings of Bickford as cited teaching a conventional bus. As a result, the assertion that the common practice is to use an input buffer with the AGPs as claimed is improper, and therefore a *prima facie* case of obviousness is not established. If the Examiner maintains such an assertion, the Applicants respectfully challenge an assertion that it is common practice to (1) include an input buffer in an AGP as claimed, (2) include a first external path as claimed, and (3) include a selector circuit as arranged in the claims. As such, Applicants respectfully request a showing of such an assertion under MPEP 2112.

Seventh, Applicants also respectfully submit that there is no motivation, other than Applicants' own specification, to combine an input buffer as claimed to an external signal path

and selector as claimed. Therefore, among other reasons, the Office Action fails to establish a *prima facie* case of obviousness. Accordingly, Applicants respectfully submit that the claims are in condition for allowance.

As to claim 21, Applicants respectfully reassert the relevant remarks made above with respect to claim 1 and again note that this claim requires, among other things, a bus bridge signal from an internal bus bridge and receiving, by an internal circuit, the bus bridge signal and further that an internal I/O circuit prevents signals from any external circuit from reaching the internal circuit. Again, as noted above, Bickford does not teach or suggest an internal I/O circuit that prevents signals from an external circuit from reaching an internal circuit, but in fact allows all external signals to pass to the AGP bus connected to the internal circuit. Instead, Bickford, as previously stated, teaches enabling and disabling the AGP graphics accelerators. As a result, the signals reach the disabled AGP graphics accelerators, thus causing the reflections sought to be avoided. Consequently, Bickford fails to teach and teaches away from "an internal I/O circuit that prevents signals from any external circuit from reaching the internal circuit." Accordingly, this claim is also believed to be in condition for allowance.

As to claim 29, Applicants respectfully reassert the relevant remarks made above with respect to claim 1 and again note that Bickford does not teach an integrated bus bridge graphics unit coupled to memory that includes an internal circuit operably configured to avoid signals from an external graphics bus. Instead, Bickford, as previously stated, teaches enabling and disabling the AGP graphics accelerators. Since Bickford teaches that the internal graphics bus is coupled directly to the external slot and to the internal AGP graphics chip (see Fig. 3), no external graphics path or bus is taught by Bickford. Bickford simply controls the receipt of a frame # signal from the PCI bus to either of the two graphics controllers to enable or disable one of the two graphics controllers. As such, this claim includes new and nonobvious subject matter and is also believed to be in condition for allowance.

The dependent claims add additional novel and nonobvious subject matter and are also allowable. For example, as to claim 2, it is alleged that the Bickford reference discloses an output buffer (structure 170) and provides a second internal signal via the first external signal path. The Office Action admits that Bickford does not disclose, among other things, a separate

second internal signal path for conveying signal to the output buffer. The Office Action, however, alleges that duplication of working parts of the device which are normally formed in two pieces is well known and that only routine skill in the computer art would be needed to add an additional internal signal path and to integrate the external output path and external input path into one external path. Applicants respectfully note that, since Bickford does not describe a first internal or a first external signal path, Bickford fails to describe the output buffer is operative to receive a second internal signal via the second internal path and to provide the second internal signal via the first external signal path as recited in claim 2. Accordingly, such a combination of internal circuit, input buffer, output buffer and selector circuit is not taught or suggested by the cited references. Further, as stated above, the references teach against such a combination as claimed.

As to claim 20, the claim requires, among other things, that the input buffer is inoperable to provide the external signal from the first external signal path to the first internal circuit and that the output buffer is inoperable to provide the first external signal from the first external signal path to the first internal circuit. This isolation is not taught or suggested by Bickford and, as such, this claim is also believed to be in condition for allowance.

Accordingly, Applicant respectfully submits that the Claims are in condition for allowance and requests that a timely Notice of Allowance be issued in this case. The Examiner is invited to contact the below-listed attorney if the Examiner believes that a telephone conference will advance the prosecution of this application.

Respectfully submitted,

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